IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

AVM TECHNOLOGIES, LLC,	)	
	)	
Plaintiff,	)	
	)	C.A. No. 10-610-RK
v.	)	
	)	
INTEL CORPORATION,	)	
	)	
Defendant.	)	

JOINT CLAIM CONSTRUCTION CHART

Pursuant to the Court's October 8, 2010 Scheduling Order, Plaintiff AVM Technologies, LLC ("AVM") and Defendant Intel Corporation ("Intel") hereby provide this joint claim construction chart.

Counsel for AVM and Intel have met and conferred in good faith according to the Court's Scheduling Order to resolve claim construction issues and to reduce the burden on the Court. Through those discussions, AVM and Intel have been able to resolve a number of issues with respect to claim construction.

Table 1 identifies claim terms for which the parties have agreed to proposed constructions. Table 2 identifies claim terms for which the parties have different proposed constructions. Table 3 identifies claim terms which Intel alleges are indefinite under 35 U.S.C. § 112, ¶ 2, and therefore are not amenable to construction. AVM disagrees with Intel regarding the claim terms in Table 3, and has provided its position on the disputed terms within the table.

Table 1: Claim Terms with Agreed-Upon Claim Constructions

Claim Term	AVM and Intel Joint Construction
"coupled to" (claims 1, 2, 4, 6, 12, 13, 16)	"connected to, directly or through intervening elements"
"coupled between" (claims 7, 12)	"connected between, directly or through intervening elements"
"couplable to" (claim 12)	"capable of being connected"
"coupling" (claim 14)	"connected, either directly or through intervening elements"
"anti-float circuit" (claims 4, 5, 16)	"a circuit used to prevent the precharge node from floating or otherwise losing the current state of the circuit"
"precharge node" (claims 12, 16)	"the output node of the dynamic logic circuit"

Table 2: Claim Terms Having Different Proposed Constructions

Claim Term	AVM Proposed Construction	Intel Proposed Construction
"a delay" (claims 1, 2, 3, 7, 12)	"circuit that delays deactivation of the precharge transistor"	no construction required
"for simultaneously activating" (claim 1)	"for causing to be on concurrently for a portion of the evaluation phase"	"for activating at the same time"

Claim Term	AVM Proposed Construction	Intel Proposed Construction
"are activated simultaneously for a period of time" (claim 19)	"are caused to be on concurrently for a portion of the evaluation phase"	"are activated at the same time for a period sufficient to overcome charge sharing between the precharge node and the dynamic logic block"
"precharge transistor" (claims 1, 2, 4, 6, 7, 9, 12, 13, 18, 19, 20, 21)	"transistor that charges a precharge node and not the logic block during the precharge phase"	"a transistor that is connected to a clock signal, rather than a data signal, and charges the precharge node"
"evaluation transistor" (claims 1, 6, 9, 12, 13, 18, 19, 20, 21)	"transistor that functions to isolate the precharge node from the logic block"	"a transistor that is connected to a clock signal, rather than a data signal, and is used to control when the precharge node may discharge"
"dynamic logic circuit" (claims 1-7, 9, 12-14, 16, 18-21)	ordinary and customary meaning, *i.e.*, "a circuit that is precharged and subsequently performs a logical function"	"a dynamic circuit that implements a logic function, rather than a memory function"
"dynamic logic block" (claims 1, 19, 20)	"block containing one or more input transistors that implements a logic function"	"a circuit block that receives data signals, rather than a clock signal, and implements the logic function of the dynamic logic circuit"
"logic block" (claim 12)	"block containing one or more input transistors that implements a logic function"	"a circuit block that receives data signals, rather than a clock signal, and implements the logic function of the dynamic logic circuit"

Table 3: Claim Terms That Intel Contends Are Not Amenable to Construction

Claim Term	Intel's Contention	AVM's Response
"during a major portion of the evaluation phase" (claim 6)	Renders claim 6 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2	One of ordinary skill in the art would understand the phrase "a major portion of the evaluation phase." *See* '547 Patent, cols. 5:44-6:50; Figs. 4A-4E; *see also, Moore U.S.A., Inc. V. Standard Register Co.*, 229 F.3d 1091 (Fed. Cir. 2000)
"during a majority of the evaluation clock phase" (claim 20)	Renders claim 20 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2	One of ordinary skill in the art would understand the phrase "a majority of the evaluation clock phase." *See* '547 Patent, cols. 5:44-6:50; Figs. 4A-4E; *see also, Moore U.S.A., Inc. V. Standard Register Co.*, 229 F.3d 1091 (Fed. Cir. 2000)
"during a major portion of an evaluation clock phase" (claim 21)	Renders claim 21 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2	One of ordinary skill in the art would understand the phrase "a major portion of an evaluation clock phase." *See* '547 Patent, cols. 5:44-6:50; Figs. 4A-4E; *see also, Moore U.S.A., Inc. V. Standard Register Co.*, 229 F.3d 1091 (Fed. Cir. 2000)
"during a minor portion of the evaluation clock phase" (claim 21)	Renders claim 21 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2	One of ordinary skill in the art would understand the phrase "a minor portion of the evaluation clock phase." *See* '547 Patent, cols. 5:44-6:50; Figs. 4A-4E; *see also, Moore U.S.A., Inc. V. Standard Register Co.*, 229 F.3d 1091 (Fed. Cir. 2000)

Claim Term	Intel's Contention	AVM's Response
"the precharge and evaluation transistors are activated simultaneously for a period of time" (claim 19)	Renders claim 19 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2. *See IPXL Holdings, Inc. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005).	AVM contends that this identified claim phrase is amendable to construction. *See* proposed constructions above for all claim terms contained within this identified phrase; *see also*, '547 Patent, col. 6:20-26; Figs. 4B, 4D, 4E

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